AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning on line 16 of page 4 and ending on line 2 of page 5 as follows:

FIG. 1 is a block diagram of a source synchronous clocking system 1 for transferring signals between a link layer 2 to a PHY layer 3. The source synchronous clocking system 1 comprises a transmit (Tx) clock domain 4 and a receive (Rx) clock domain 7 in the link layer 2, and a transmit clock domain 5 and a receive clock domain 6 in the PHY layer 3. The link layer 2 comprises an ATM layer or a frame layer. From the link layer 2 to the PHY layer 3, the following signals are transferred: a transmit clock 8, a transmit control 9, a transmit data 10, and a receive flow control 11. From the PHY layer 3 to the link layer 2, the following signals are transferred: a receive clock 14, a receive control 15, a receive data 16, and a ~~transmit control 17~~ transmit flow control 60.